

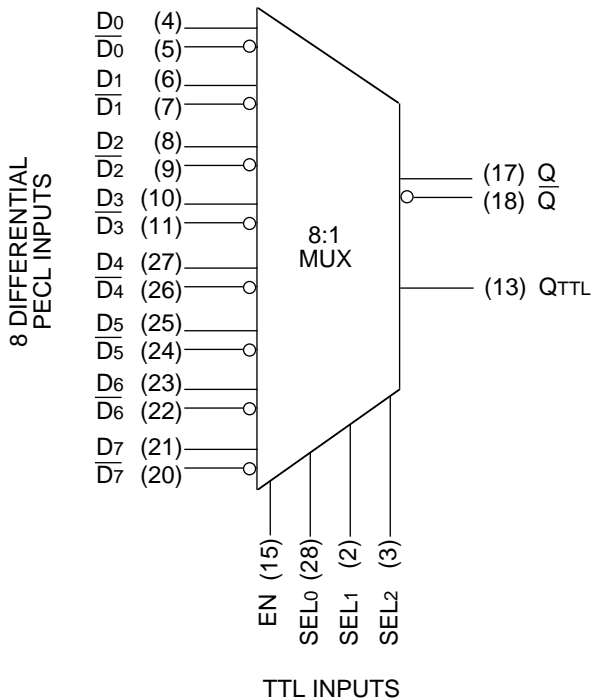
FEATURES

- Low skew
- Differential PECL inputs
- Differential cut-off PECL outputs capable of driving 25Ω load for driving data bus
- Tri-state TTL output
- TTL select and enable input
- Internal 75KΩ PECL input pull-down resistors
- PECL I/O fully compatible with industry standard
- Available in 28-pin PLCC package

DESCRIPTION

The SY100S863 is a PECL 8:1 multiplexer designed for use in new, high-performance PECL systems. It has differential PECL outputs and a standard TTL output. The TTL select inputs (SEL₀, SEL₁, SEL₂) determine which one of the eight differential PECL data inputs (D₀–D₇) is propagated to the outputs. The enable pin, EN, is provided for expansion. When EN is at a TTL logic one level, both PECL and TTL outputs are enabled. When the enable pin is set to TTL logic zero level, both PECL outputs of the differential pair are in cut-off and the TTL output is in a three-state condition.

BLOCK DIAGRAM

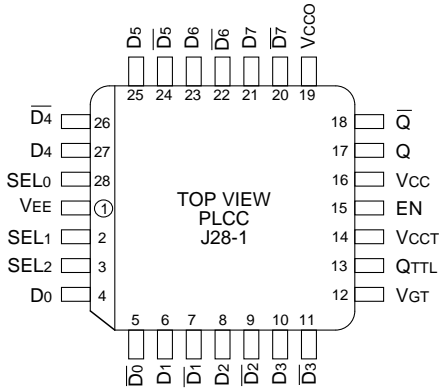


PIN NAMES

Pin	Function
D ₀ , /D ₀ – D ₇ , /D ₇	Differential PECL Input Pairs
Q, /Q	Differential PECL Outputs
QTTL	TTL Output
EN	Enable Input
SEL _{0,1,2}	Select Inputs

PACKAGE/ORDERING INFORMATION

Ordering Information



28-Pin PLCC (J28-1)

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S863JC	J28-1	Commercial	SY100S863JC	Sn-Pb
SY100S863JCTR ⁽¹⁾	J28-1	Commercial	SY100S863JC	Sn-Pb
SY100S863JZ ⁽²⁾	J28-1	Commercial	SY100S863JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S863JZTR ^(1, 2)	J28-1	Commercial	SY100S863JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

TRUTH TABLE

EN	SEL ₂	SEL ₁	SEL ₀	Q	QTTL
H	L	L	L	D ₀	D ₀
H	L	L	H	D ₁	D ₁
H	L	H	L	D ₂	D ₂
H	L	H	H	D ₃	D ₃
H	H	L	L	D ₄	D ₄
H	H	L	H	D ₅	D ₅
H	H	H	L	D ₆	D ₆
H	H	H	H	D ₇	D ₇
L	X	X	X	Z	Z

PECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = V_{CCO} = V_{CC_T} = 5.0V ± 5%; V_{EE} = V_{GT} = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V _{OH}	Output HIGH Voltage ⁽¹⁾	3.975	4.045	4.13	V	Loading with 25Ω to 3V (V _{CC} -2V)
V _{OL}	Output LOW Voltage ⁽¹⁾	3.17	3.295	3.38	V	Loading with 25Ω to 3V (V _{CC} -2V)
V _{OZ}	Cutoff Voltage ⁽¹⁾	—	3	3.10	V	Loading with 25Ω to 3V (V _{CC} -2V)
V _{IH}	Input HIGH Voltage	3.835	—	4.13	V	
V _{IL}	Input LOW Voltage	3.17	—	3.525	V	
I _{IH}	Input HIGH Current	—	—	350	μA	V _{IN} = V _{IH} (Max.)
I _{IL}	Input LOW Current	0.50	—	—	μA	V _{IN} = V _{IL} (Min.)
I _{CC}	V _{CC} Supply Current	—	73	88	mA	

Note:

1. Levels shown are for V_{CCO} = 5.0V and will vary 1:1 with powers.

TTL DC ELECTRICAL CHARACTERISTICS

V_{CC} = V_{CCO} = V_{CC_T} = 5.0V ± 5%; V_{EE} = V_{GT} = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V _{OH}	Output HIGH Voltage	2.4	2.9	—	V	I _{OH} = -3mA
V _{OL}	Output LOW Voltage	—	0.3	0.5	V	I _{OL} = 24mA
V _{IH}	Input HIGH Voltage	2.0	—	V _{CC}	V	
V _{IL}	Input LOW Voltage	0	—	0.8	V	
I _{IH}	Input HIGH Current	—	—	1.0	mA	V _{IN} = 2.7V
I _{IL}	Input LOW Current	-0.7	—	—	mA	V _{IN} = 0.5V
V _{IK}	Input Clamp Voltage	-1.2	—	—	V	I _{IN} = -18mA
I _{OS}	Output Short Circuit Current	-200	—	-60	mA	V _{OUT} = 0V, V _{CC_T} = 5.5V
I _{OZHT}	Tri-state Current Output HIGH	—	—	70	μA	V _{OUT} = 2.7V
I _{OZLT}	Tri-state Current Output LOW	-700	—	—	μA	V _{OUT} = 0.5V

PECL AC ELECTRICAL CHARACTERISTICS

VCC = VCCO = +5.0V ± 5%; VEE = VGT = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
tPLH tPHL	Propagation Delay ^{(1),(2)} D to Q SEL0 to Q SEL1 to Q SEL2 to Q	500	—	900	500	—	900	500	—	900	ps	
tPZH tPHZ	EN to Q ⁽³⁾ (Cutoff to HIGH) EN to Q ⁽³⁾ 300 (HIGH to Cutoff)	300	—	1750	300	—	1750	300	—	1750	ps	
tr tf	Output Rise/Fall Times ⁽²⁾ 20% to 80%	300	400	600	300	400	600	300	400	600	ps	

Notes:

1. Part-to-part skew is defined as Max. – Min. value at the given temperature.
2. RL = 50Ω
3. Figures 1 and 2

TTL AC ELECTRICAL CHARACTERISTICS

VCC = VCCO = 5V ± 5%; VEE = VGT = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
tPLH tPHL	Propagation Delay ^{(1),(2)} D to QTTL SEL0 to QTTL SEL1 to QTTL SEL2 to QTTL	2.5	—	5.0	2.5	—	5.0	2.5	—	5.0	ns	
tPZH tPZL	EN to TTL Output ⁽²⁾ (Enable Time)	2.5	—	5.0	2.5	—	5.0	2.5	—	5.0	ns	
tPHZ tPLZ	EN to TTL Output ⁽²⁾ (Disable Time)	2.5	—	5.0	2.5	—	5.0	2.5	—	5.0	ns	
tr tf	Output Rise/Fall Time ⁽³⁾ 0.8V to 2.4V 0.8V to 2.0V	0.3	—	1.6	0.3	—	1.6	0.3	—	1.6	ns	

Notes:

1. Part-to-part skew is defined as Max. – Min. value at the given temperature.
2. Figures 3 and 4
3. CL = 25pF

PECL-TO-PECL TEST CIRCUITRY

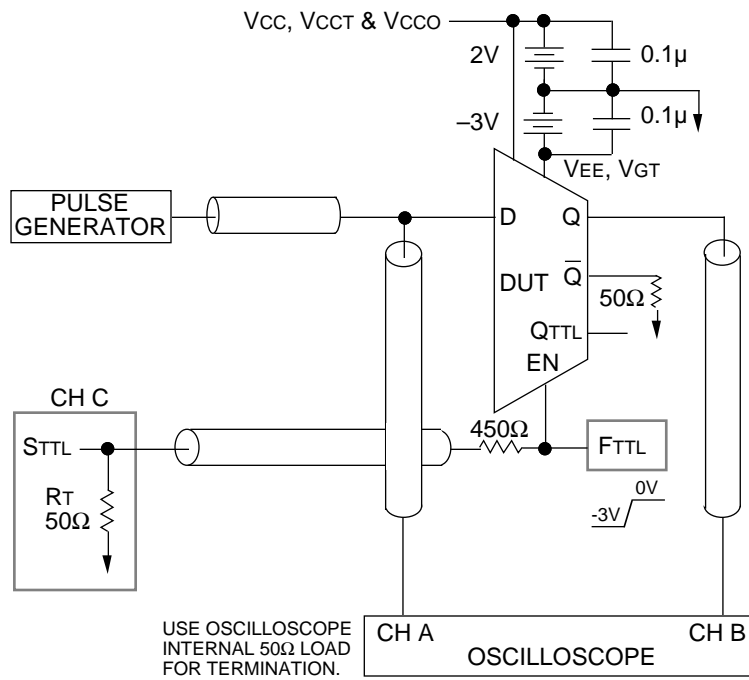


Figure 1. PECL-to-PECL AC Test Circuit

PECL-TO-PECL SWITCHING WAVEFORMS

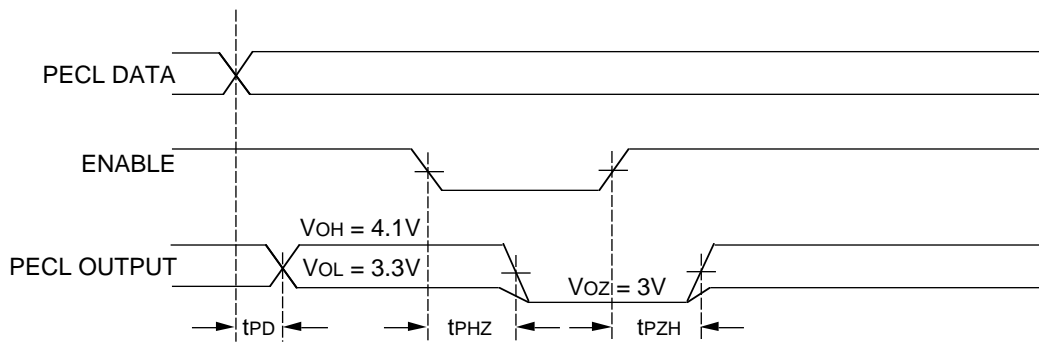


Figure 2. PECL-to-PECL Transition — Propagation Delay and Transition Times

PECL-TO-TTL TEST CIRCUITRY

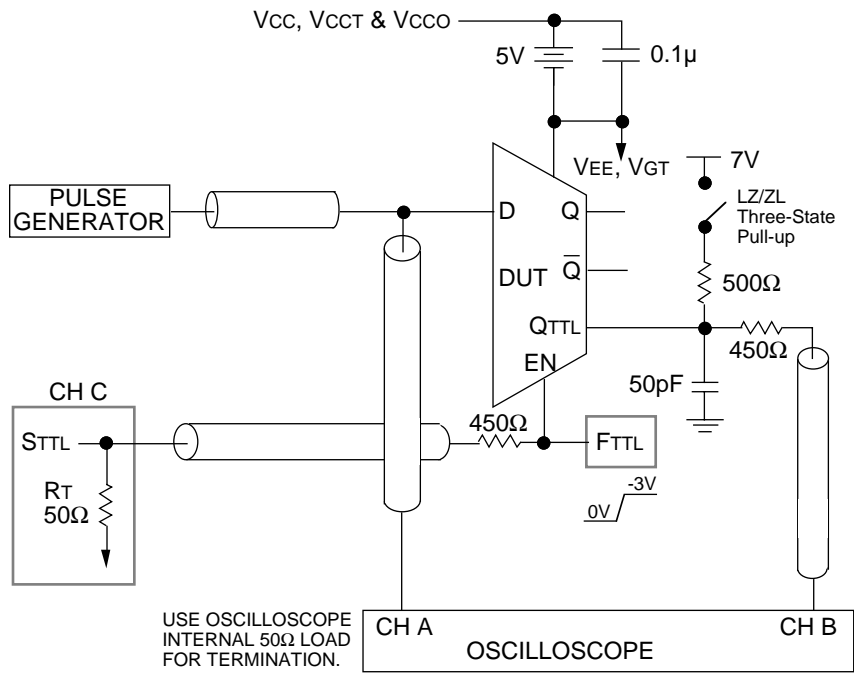


Figure 3. PECL-to-TTL AC Test Circuit

PECL-TO-TTL SWITCHING WAVEFORMS

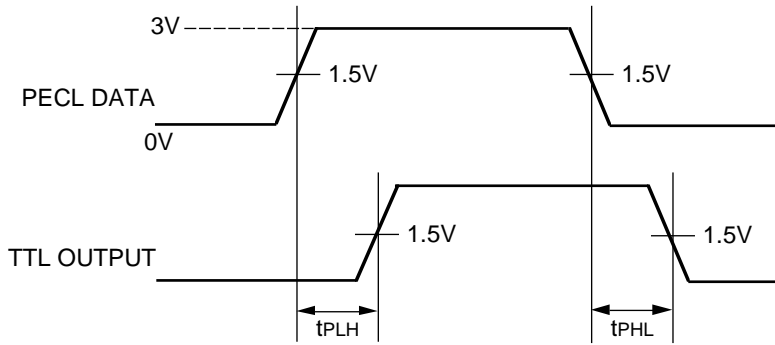


Figure 4a. PECL-to-TTL Transition, Data to TTL Output Delay

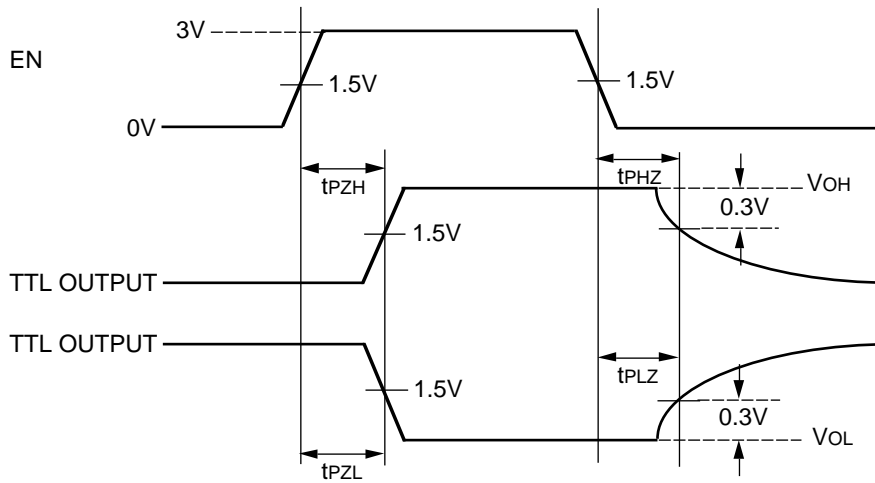
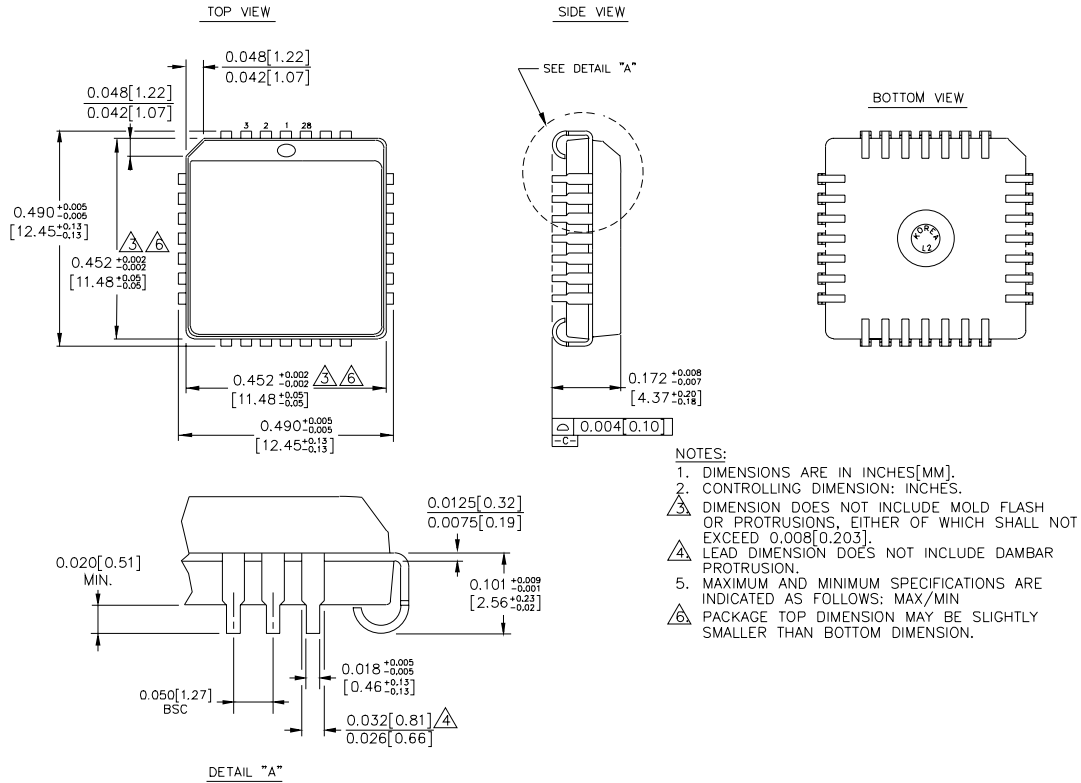


Figure 4b. EN to TTL Output Enable and Disable Times

28-PIN PLCC (J28-1)



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